WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a memory block including a ferroelectric memory;

a peripheral circuit that controls access to the memory block; and

a data destruction unit that stops an operation for writing back destructed data to an area of the memory block in which data is destructed by a data read operation for the memory block.

2. The semiconductor memory device according to claim 1, wherein the data destruction unit includes a plate line control circuit that lowers an electric potential of a plate line after a bit line is pre-charged with a ground potential.

3. The semiconductor memory device according to claim 2, further comprising:

a switching unit for determining from an outside whether the plate line control circuit should lower the electric potential of the plate line before the bit line is pre-charged with the ground potential or after the bit line is pre-charged with the ground potential.

4. The semiconductor memory device according to claim 3, wherein the switching unit is operated in response to a control signal input from the outside.

5. The semiconductor memory device according to claim 1, further comprising:

a boost stopping unit that stops an operation for boosting a voltage of the word line to a write voltage while the plate line control circuit lowers the electric potential of the plate line after the bit line is pre-charged with the ground potential.

6. The semiconductor memory device according to claim 5, wherein the boost stopping unit is a boost control circuit that controls an electric potential of a coupling capacitance connected to the word line.

7. The semiconductor memory device according to claim 5, further comprising:

a switching unit that determines from the outside whether the boost control circuit stops boosting the voltage of the word line.

8. The semiconductor memory device according to claim 7, wherein the switching unit is operated in response to a control signal input from the outside.

9. The semiconductor memory device according to claim 1, further comprising:

a data output stopping unit that stops output of the data read from the memory block to the outside.

10. The semiconductor memory device according to claim 9, wherein the data output stopping unit is a clamp circuit that clamps the bit line to a predetermined potential.

11. The semiconductor memory device according to claim 10, further comprising:

a switching unit that determines whether the clamp circuit is to clamp the bit line with the predetermined potential from the outside.

12. The semiconductor memory device according to claim 11, wherein the switching unit is operated in response to a control signal input from the outside.

13. The semiconductor memory device according to claim 9, further comprising:

a sensing stopping unit that stops an operation of a sense amplifier for amplifying the electric potential of the bit line.

14. The semiconductor memory device according to claim 13, further comprising:

a switching unit that determines whether the sensing stopping unit is to stop the operation of the sense amplifier, from the outside.

15. The semiconductor memory device according to claim 14, wherein the switching unit is operated in response to a control signal

input from the outside.

16. The semiconductor memory device according to claim 1, further comprising:

a multiple-select unit that simultaneously raises potentials of two word lines having a combination with a same plate line.

17. The semiconductor memory device according to claim 16, wherein the multiple-select unit comprises a switching unit that determines from the outside whether to simultaneously raise the potentials of the two word lines having a combination with the same plate line.

18. The semiconductor memory device according to claim 17, wherein the switching unit is operated in response to a control signal input from the outside.

19. A semiconductor memory device comprising:

a memory block including a ferroelectric memory;

a peripheral circuit that controls access to the memory block;

a data destruction unit that stops an operation for writing back destructed data to an area of the memory block in which data is destructed by a data read operation for the memory block, wherein the data destruction unit includes a plate line control circuit that lowers an electric potential of a plate line after a bit line is pre-charged with a

ground potential;

a first switching unit that determines from an outside whether the plate line control circuit should lower the electric potential of the plate line before the bit line is pre-charged with the ground potential or after the bit line is pre-charged with the ground potential, wherein the first switching unit is operated in response to a first control signal input from the outside;

a boost stopping unit that stops an operation for boosting a voltage of the word line to a write voltage while the plate line control circuit lowers the electric potential of the plate line after the bit line is pre-charged with the ground potential;

a second switching unit that determines from the outside whether the boost control circuit stops boosting the voltage of the word line, wherein the second switching unit is operated in response to a second control signal input from the outside;

a data output stopping unit that stops output of the data read from the memory block to the outside, wherein the data output stopping unit is a clamp circuit that clamps the bit line to a predetermined potential;

a third switching unit that determines whether the clamp circuit is to clamp the bit line with the predetermined potential from the outside, wherein the third switching unit is operated in response to a third control signal input from the outside;

a sensing stopping unit that stops an operation of a sense amplifier for amplifying the electric potential of the bit line;

a fourth switching unit that determines whether the sensing stopping unit is to stop the operation of the sense amplifier, from the outside, wherein the fourth switching unit is operated in response to a fourth control signal input from the outside; and

a multiple-select unit that simultaneously raises potentials of two word lines having a combination with a same plate line, wherein the multiple-select unit comprises a fifth switching unit that determines from the outside whether to simultaneously raise the potentials of the two word lines having a combination with the same plate line, wherein the fifth switching unit is operated in response to a fifth control signal input from the outside,

wherein the first control signal, the second control signal, the third control signal, the fourth control signal, and the fifth control signal are same signals.